

Appl. No. 10/625,505
Amdt. dated August 18, 2006
Reply to Office Action of May 19, 2006

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method in a computer system for compiling a design for an integrated circuit, the method comprising:
~~automatically performing multiple compilations of the design using a series of values for each input parameter in a set of input parameters for the design, each input parameter corresponding to a controllable aspect of the design, to generate output values for one or more output metrics based on the series of values, each output metric corresponding to a variable parameter of the integrated circuit to be tracked or optimized during the compiling, the series of values including random values that are automatically selected for the multiple compilations;~~
~~reporting the output values for the output metrics; and~~
concluding the performing of multiple compilations when an output value for at least one of the output metrics reaches a pre-selected stopping criteria; and has been reached;
determining optimal values for the input parameters based on the multiple compilations, the optimal values operable to be used to synthesize the design.
~~wherein the method produces a table of results of the output metrics for each combination of input parameters used for a compilation.~~
2. (Canceled).
3. (Original) The method according to claim 1 wherein:
the method produces a signature of the best configuration of input parameters, for use in future compilations.
4. (Currently Amended) A method in a computer system for compiling a design for an integrated circuit, the method comprising:
~~automatically performing multiple compilations of the design using a series of values for each input parameter in a set of input parameters for the design, each input parameter~~

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corresponding to a controllable aspect of the design, to generate output values for one or more output metrics based on the series of values, each output metric corresponding to a variable parameter of the integrated circuit to be tracked or optimized during the compiling, the series of values including random values that are automatically selected for the multiple compilations; reporting the output values for the output metrics; and concluding the performing of multiple compilations when an output value for at least one of the output metrics reaches a pre-selected stopping criteria; and has been reached, determining wherein the method produces a metric of average results for the output metrics across a range of input parameters used for the multiple compilations to indicate expected noise or variability for the design.

5. (Currently Amended) The method according to claim 4 wherein:
the metric is average results are used to distinguish gains in the design due to the input parameters from random fluctuation in the gains.

6. (Original) The method according to claim 1 wherein:
one of the input parameters is a random seed or initial configuration parameter.

7. (Currently Amended) The method according to claim 1 wherein:
one of the input parameters is an effort level for the compilation tool or a portion of the compilation tool.

Claims 8-10. (Canceled).

11. (Currently Amended) A method in a computer system for compiling a design for an integrated circuit, the method comprising:
automatically performing multiple compilations of the design using a series of values for each input parameter in a set of input parameters for the design, each input parameter corresponding to a controllable aspect of the design, to generate output values for one or more output metrics based on the series of values, each output metric corresponding to a variable

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parameter of the integrated circuit to be tracked or optimized during the compiling, the series of values including random values that are automatically selected for the multiple compilations;
~~reporting the output values for the output metrics; and~~
concluding the performing of multiple compilations when an output value for at least one of the output metrics reaches a pre-selected stopping criteria; and has been reached,
determining optimal values for the input parameters based on the multiple compilations, the optimal values operable to be used to synthesize the design,

wherein at least one of the input parameters: defines a level of effort to a register packing algorithm that combines circuit elements in the design into fewer logic elements on the integrated circuit when enabled; is a balancing parameter to technology mapping in synthesis; adds or deletes one optimization algorithm or step from a default CAD flow, or modifies an order in which CAD steps are applied to the integrated circuit; is a choice or specification of an alternate synthesis optimization script; or enables a netlist optimization or physical resynthesis step.

Claims 12-15. (Canceled).

16. (Previously Presented) A method in a computer system for compiling a design for an integrated circuit, the method comprising:

~~automatically performing multiple compilations of the design using a series of values for each input parameter in a set of input parameters for the design, each input parameter corresponding to a controllable aspect of the design, to generate output values for one or more output metrics based on the series of values, each output metric corresponding to a variable parameter of the integrated circuit to be tracked or optimized during the compiling, the series of values including random values that are automatically selected for the multiple compilations;~~
~~reporting the output values for the output metrics; and~~
concluding the performing of multiple compilations when an output value for at least one of the output metrics reaches a pre-selected stopping criteria; and has been reached,
determining optimal values for the input parameters based on the multiple compilations, the optimal values operable to be used to synthesize the design,

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wherein the output metrics include at least one of: a measure of the longest delay path in the design; a quantification of logic area or other resource usage of the integrated circuit; an estimate of power consumption; and a metric for a number of paths, register-register pairs, IO-register pairs, or register-IO pairs that fail to meet a specified timing constraint.

Claims 17-19. (Canceled).

20. (Original) The method according to claim 1 wherein:
 the set of output metrics includes a minimum slack calculated on the integrated circuit.

21. (Original) The method according to claim 1 wherein:
 the set of output metrics includes a total slack calculated on the integrated circuit.

22. (Currently Amended) A method in a computer system for compiling a design for an integrated circuit, the method comprising:
automatically performing multiple compilations of the design using a series of values for each input parameter in a set of input parameters for the design, each input parameter corresponding to a controllable aspect of the design, to generate output values for one or more output metrics based on the series of values, each output metric corresponding to a variable parameter of the integrated circuit to be tracked or optimized during the compiling, the series of values including random values that are automatically selected for the multiple compilations;

~~reporting the output values for the output metrics; and~~
concluding the performing of multiple compilations when an output value for at least one of the output metrics reaches a pre-selected stopping criteria; and has been reached,
determining optimal values for the input parameters based on the multiple compilations, the optimal values operable to be used to synthesize the design,
 wherein the stopping criteria for the method is based on at least one of: exhausting all possible combination of specified input parameters independent of results; a total compile

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time consumed over all of the compilations thus far; the number of failing timing paths in the circuit; and a statistical calculation of possible success by the method.

23. (Original) The method according to claim 1 wherein:
the stopping criteria is based on achieving a user's specified constraints.
24. (Canceled).
25. (Original) The method according to claim 1 wherein:
the stopping criteria is based on a number of failed constraints in the integrated circuit.
26. (Canceled).
27. (Original) The method according to claim 1 wherein:
the stopping criteria is based on achieving a minimum worst-case slack in the integrated circuit.
28. (Original) The method according to claim 1 wherein:
the stopping criteria is based on a total slack in the circuit.
29. (Canceled).
30. (Currently Amended) The method according to claim 1 wherein:
~~automatically~~ performing multiple compilations includes using a static schedule pre-calculated by a tool to select the series of values for each input parameter to be used in the compilations.
31. (Currently Amended) The method according to claim ~~[[1]]~~ 30 wherein:
the static schedule is dynamically modified based on a metric of current distance from the user goals.

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32. (Currently Amended) A computer ~~system~~ program product embedded in a computer readable medium for automating compilation of a design for an integrated circuit, ~~the method comprising:~~

computer program code for automatically performing multiple compilations of the design using a series of values for each input parameter in a set of input parameters for the design, each input parameter corresponding to a controllable aspect of the design, to generate output values for one or more output metrics based on the series of values, each output metric corresponding to a variable parameter of the integrated circuit to be tracked or optimized during the compiling, the series of values including random values that are automatically selected for the multiple compilations;

~~for reporting the output values of the output metrics; and~~

computer program code for concluding the performing of multiple compilations when an output value for at least one of the output metrics reaches a pre-selected stopping criteria; and has been reached;

computer program code for determining optimal values for the input parameters based on the multiple compilations, the optimal values operable to be used to synthesize the design.

~~wherein the code for reporting the output values further comprises code for producing a table of results of the output metrics for each combination of input parameters used for a compilation.~~

33. (Canceled).

34. (Currently Amended) The computer ~~system~~ program product according to claim 32 further comprising:

computer program code for producing a signature of the best configuration of input parameters, for use in future compilations.

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35. (Currently Amended) A computer ~~system~~ program product embedded in a computer readable medium for automating compilation of a design for an integrated circuit, the method comprising:

computer program code for automatically performing multiple compilations of the design using a series of values for each input parameter in a set of input parameters for the design, each input parameter corresponding to a controllable aspect of the design, to generate output values for one or more output metrics based on the series of values, each output metric corresponding to a variable parameter of the integrated circuit to be tracked or optimized during the compiling, the series of values including random values that are automatically selected for the multiple compilations;

~~for reporting the output values of the output metrics; and~~

computer program code for concluding the performing of multiple compilations when an output value for at least one of the output metrics reaches a pre-selected stopping criteria; and has been reached; and

computer program code for determining producing a metric of average results for the output metrics across a range of input parameters used for the multiple compilations to indicate expected noise or variability for the design.

36. (Currently Amended) The computer ~~system~~ program product according to claim 35 wherein the ~~metric is~~ average results are used to distinguish gains due to the input parameters from random fluctuation.

37. (Currently Amended) The computer program product method according to claim 32 wherein:

one of the input parameters is a random seed or initial configuration parameter.

38. (Currently Amended) The computer program product method according to claim 32 wherein:

one of the input parameters is an effort level for the compilation tool or a portion of the compilation tool.

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Claims 39-40. (Canceled)

41. (New) The method according to claim 1 wherein:
the method produces a table of results of the output metrics for each combination
of input parameters used for a compilation.

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